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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,808	08/28/2003	Klaas Bult	1875.0510002	5778

26111 7590 08/05/2005

STERNE, KESSLER, GOLDSTEIN & FOX PLLC
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
LAM, TUAN THIEU	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,808	BULT ET AL.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the amendment filed 7/7/2005. Claims 1-20 are pending and are under examination.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Dhong et al. (USP 4,816,706), newly cited prior art.

Figure 8 shows a rest circuit for a latch circuit (18, 20) having a bistable pair of transistors connected to a supply voltage (VDD, ground), the reset circuit comprising a first transistor (24) connected to the supply voltage at a first terminal of said first transistor , a second transistor (48 on the left) connected between a second terminal of the first transistor and a first port of the latch (BITLINE), wherein a gate terminal of said second transistor is connected to a drain terminal of said second transistor at said first port; and a third transistor (48 on the right) connected between second terminal of said first transistor and a second port of the latch circuit (BITLINE/), wherein a gate terminal of said third transistor is connected to a drain terminal of said third transistor at said second port; wherein transistors of said latch circuit, said first transistor, said second transistor, and said third transistor are all NMOSFET as called for in claims 13-14.

3. Claims 7 and 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Opris et al. (USP 6,060,912), newly cited prior art.

Figure 1 of Opris et al. shows a latch circuit comprising a bistable pair of transistors (M15, M25) connected between a reset switch (M14) and a first supply voltage (ground), and having a first port for receiving a first current signal (I1) and producing a first output voltage, and a second port for receiving a second current signal (I2) and producing a second output voltage, and a vertical latch (M12m M13, M22, M23, INV1, INV2, NAND1, NAND2) connected between said first supply voltage and a second supply voltage (VDD), and connected to said first port, wherein said vertical latch comprises a first current mirror pair (M12, M13) connected to said bistable pair of transistors and a second current mirror pair (M22, M23) connected to said first current mirror pair to the second supply voltage as called for in claim 7.

Regarding claim 9, figure 1 shows M14 as micromechanical reset switch.

Regarding claim 10, the vertical latch is capable of decreasing the time necessary for said first port to reach a steady stage voltage in response to said first current signal received.

Regarding claim 11, figure 1 further shows a vertical reset switch (M24) connected to said vertical latch.

Regarding claim 12, figure 1 further shows a second vertical latch (M24) connected between said first supply and said second supply voltage and connected to said second port.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 15-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Ang et al. (USP 6,147,515), prior art of record. Figure 2 of Ang et al. shows a comparator comprising analog input signal (Pad), a reference signal (REF), digital output signal (Out), said comparator comprising a latch circuit (224, 226, 228, 229) having a bistable pair of transistors (226, 229) coupled between a reset circuit (209) and a first supply voltage (ground), and a vertical latch (231, 233, 235, 237, 244-247) coupled between said first power supply and a second power supply (VCC) and coupled to said bistable pair of transistors at a node coupled to said reset circuit, said vertical latch having a first transistor (244), a second transistor (245) said first transistor being a first channel type (p type), said second transistor being of a second channel type (n type) as called for in claims 15-16.

5. Claims 1-6 and 17-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Ang et al. (USP 6,147,515), prior art of record.

Figure 2 of Ang et al. shows a latch circuit comprising a bistable pair of transistors (226, 229) connected between a reset switch (209) and a first supply voltage (ground), and having a first port (SENS) for receiving a first current signal (current flows along the transistors 264, 265 to node SENS) and producing a first output voltage, and a second port (SENSB) for receiving a second current signal (current flows along the transistors 275 and 274) and producing a second output voltage, and a vertical latch (233, 235, 244 and 247) connected between said first supply voltage and a second supply voltage (Vdd and ground), and connected to said first port, said vertical latch having a transistor (244) connected to first supply (ground) but isolated from said second supply voltage when transistor 245 is off, wherein said transistor (244) is configured to

amplify a change in said first output voltage in response to said first current signal received as called for in claim 1.

Regarding claim 2, said transistor is a MOSFET.

Regarding claim 3, the reset switch 280 is a microelectromechanical reset switch.

Regarding claim 4, the vertical latch is capable of decreasing the time necessary for said first port to reach a steady stage voltage in response to said first current signal received.

Regarding claim 5, figure 2 further shows a vertical reset switch (234) connected to said vertical latch.

Regarding claim 6, figure 2 further shows a second vertical latch (231, 237, 245, 246) connected between said first supply and said second supply voltage and connected to said second port.

Regarding claim 17, figure 2 of Ang et al. is capable of amplifying the current signal received at a first latch circuit port (SENSB) while maintaining a current less than the bias current received at a second latch circuit port (SENS), applying said amplified current signal to latch circuit port receiving the current signal greater than the bias current.

Regarding claim 18, figure 2 of Ang shows a latch circuit having a bistable pair wherein the bistable pair has first and second transistors (226, 229) and a vertical latch having a third and fourth transistors (244, 247) configured so that a second terminal of the third transistor (244) is connected to a second terminal of the second transistor (226) via transistor 233, a third terminal of the third transistor is connected to a first supply voltage (VDD), a third terminal of the fourth transistor (247) is connected to a second supply voltage (ground), and a second terminal of the fourth transistor is connected to a first terminal of the third transistor, a method for reducing the

power consumed by the latch circuit, comprising the steps of resetting the bistable pair and vertical latch using reset switch (209), holding the fourth transistor (247) off during resetting.

Regarding claim 19, figure 2 of Ang further comprising steps of holding the third transistor (244) off during said setting.

Regarding claim 20, after said setting, holding the fourth transistor off when the second transistor 266 changes state from on to off.

6. Claims 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Shiratake (USP 6,147,514), prior art of record.

Regarding claim 18, figure 11 of Shiratake shows a latch circuit having a bistable pair wherein the bistable pair has first and second transistors (MX2, MX1) and a vertical latch having a third and fourth transistors (MP4, Mn5) configured so that a second terminal of the third transistor (Mp4) is connected to a second terminal of the second transistor (MX1) via transistor Mn1, a third terminal of the third transistor is connected to a first supply voltage (Vcc), a third terminal of the fourth transistor (Mn5) is connected to a second supply voltage (ground), and a second terminal of the fourth transistor is connected to a first terminal of the third transistor, a method for reducing the power consumed by the latch circuit, comprising the steps of resetting the bistable pair and vertical latch using reset switch (Mp3), holding the fourth transistor (Mn5) off during resetting.

Regarding claim 19, figure 2 of Ang further comprising steps of holding the third transistor (Mp4) off during said setting.

Regarding claim 20, after said setting, holding the fourth transistor off when the second transistor MX1 changes state from on to off.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Opris et al. (USP 6,060,912).

Figure 1 of Opris et al. shows a latch circuit comprising a bistable pair of transistors (M15, M25) connected between a reset switch (M14) and a first supply voltage (ground), and having a first port for receiving a first current signal (I1) and producing a first output voltage, and a second port for receiving a second current signal (I2) and producing a second output voltage, and a vertical latch (M12m M13, M22, M23, INV1, INV2, NAND1, NAND2) connected between said first supply voltage and a second supply voltage (VDD), and connected to said first port, wherein said vertical latch comprises a first current mirror pair (M12, M13) connected to said bistable pair of transistors and a second current mirror pair (M22, M23) connected to said first current mirror pair to the second supply voltage.

What not shown in Opris et al. is the current gain of the first curent mirror is less than as called for in claim 8. However, it is notoriously well known in the art that the gain of a current mirror circuit is determined by ratio of the transistors size of the current mirror. Dependent upon a particular application, the ratio of the transistor size is adapted to vary. Thus, varying transistor

size to obtain a specific curent gain is an obvious modification in a current mirror art. Therefore, outside of non-obvious results, the obviousness of modifying size of the transistors of the first current mirror circuit to obtain a gain of less than one will not be patentable under 35USC 103(a).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P. CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

8/3/2005